Design of Linear Feedback Shift Register using Reversible Logic

Manjunath T P[1], Deepa N[2], Praveen J[3], Raghavendra Rao[4]

M.Tech Student, Dept. of ECE, Alva's Institute of Engg & Technology, Mijar, Moodbidri, Karnataka, India[1]

Assistant Professor, Dept. of ECE, Alva's Institute of Engg &Tech, Mijar, Moodbidri, Karnataka, India[2]

Sr. Associate Professor, Dept. of ECE, Alva's Institute of Engg &Tech, Mijar, Moodbidri, Karnataka, India[3, 4]

Abstract: Reversible logic is playing an important role in research areas and has found its applications in low power CMOS VLSI, Nanotechnology and Quantum computation. Recently, several researchers have focused their efforts on the design and synthesis of efficient reversible logic circuits. LFSR's are attractive structures in the area of digital system testing and fault tolerant computing. In this work, we present designs of reversible LFSR using D flip flops with asynchronous set/reset. The comparison of proposed design is done in terms of the quantum cost, delay and garbage out puts. The important reversible gates used for Reversible logic design are Feynman gate, Fredkin gate, Toffoli gate, SAM gate etc.

Keywords: Low-power VLSI, Low-power CMOS design, reversible logic, LFSR.

I. INTRODUCTION

Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. With the number of chip components doubling every 18 months, as per Moore's Law, the Irreversible Technologies would dissipate a lot of heat and reduce circuit life. It is here the Reversible Logic comes into action in not only recovering the lost information but also dissipating less heat. Landauers principle states that logic computations that are not reversible necessarily generates KT*log2 joules of heat energy for every bit of information that is lost, where k is the Boltzmann's constant and T is the absolute temperature at which the computation is performed. For room temperature T, the amount of dissipating heat is small (2.9x10-21 joules) but not negligible [1].

Bennett showed that KTln2 energy dissipation would not occur if computation is carried out in a reversible way [2]. In the year 1994 Shor [5] did a remarkable research work in creating an algorithm using reversibility for factorizing large number with better efficiency when compared to the classical computing theory. After this the work on reversible computing has been started by more people in different fields such as nanotechnology, quantum computers and CMOS VLSI.

Reversible logic is being considered as an alternative of traditional irreversible logic as reversible computing does not erase or lose any information hence the reversible logic has a theoretical potential to dissipate no energy. Reversible circuits are designed using reversible logic gates that have the same number of inputs and outputs and have one-to-one mapping between inputs and outputs; thus, the input states can be always reconstructed from the output states [7]. A gate (circuit) is reversible if it maps each input assignment to a unique output assignment, that is, if the mapping of inputs to outputs is objective. Thus, the number of inputs and outputs in a reversible gate or circuit are equal. The N*N reversible gate can be represented as shown in Figure 1.
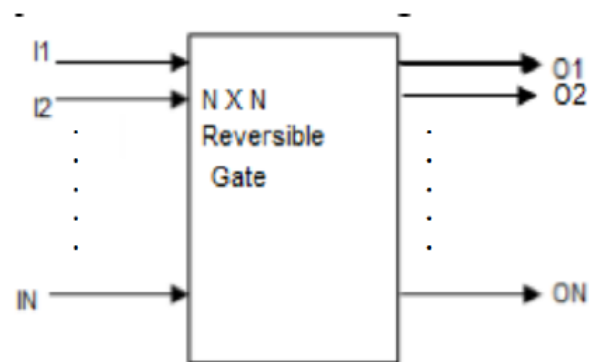

FIG 1: N*N Reversible logic

Recently, the design of reversible sequential circuits has also attracted the attention of researchers such as the work in [4, 9, 12, 13].

2. BASIC DEFINITIONS RELATED TO REVERSIBLE LOGIC

Definition 2.1: The function f(x1, x2 … xn) of n Boolean variables is called reversible if: 1. The number of outputs is equal to the number of inputs. 2. Any input pattern maps to a unique output pattern. In other words, the output of a reversible function is a permutation of the set of its inputs [14].

Definition 2.2: For an (n, k) function, i.e. function with n-input k-output, it is necessary to add inputs and/or outputs to make it reversible. "Garbage" is the number of outputs added to make an (n, k) function reversible. While the word "constant inputs" is used to denote the pre-set value inputs that were added to an (n, k) function to make it reversible. The constant inputs are known as ancillary inputs[14].The relation between garbage outputs and constant inputs is Input + constant input= output + garbage

Definition 2.3: Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of any 2*2 gate is the same, which is 1 [18].

Definition 2.4: The Delay of a Reversible Logic Gate is the maximum number of gates in a path from any input line to its corresponding output line.

3. BASIC REVERSIBLE LOGIC GATES

There are many number of reversible logic gates that exist at present. The quantum cost of each reversible logic gate is an important optimization parameter [16]. The quantum cost of a 1x1 reversible gate is assumed to be zero while the quantum cost of a 2x2 reversible logic gate is taken as unity. The quantum cost of other reversible gates is calculated by counting the number of V, V+ and CNOT gates present in their circuit. V is the square root of NOT gate and V+ is its Hermitian. The V and V+ quantum gates have the following properties:

$$V * V = NOT \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$
$$V * V+ = V+ * V = 1 \quad \ldots\ldots\ldots\ldots\ldots \quad (2)$$
$$V+ * V+ = NOT \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (3)$$

Some of the important reversible logic gates are

1) NOT Gate
The simplest Reversible gate is NOT gate and is a 1*1 gate [7]. The Reversible 1*1 gate is NOT Gate with zero Quantum Cost. It is as shown in the Figure 3.1 Input Vector = A, Output
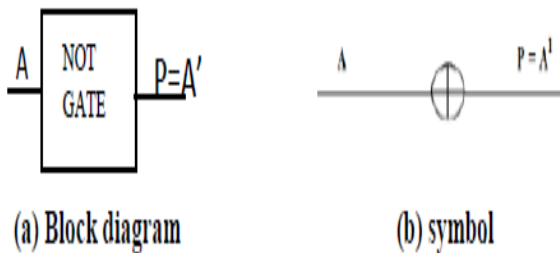
Vector=A'
FIG 3: Not gate

2) CNOT /Feynman Gate:
Feynman gate [17]is also known as controlled-not gate (CNOT). It is a 2*2 reversible gate with Quantum cost of 1. The CNOT or Feynman gate can be described as: Input Vector = (A, B) Output Vector=A XOR B As shown in Figure 4
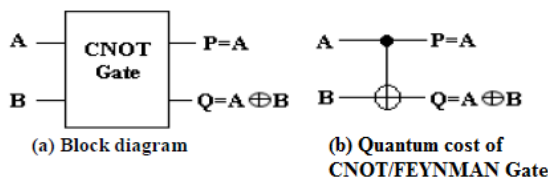

FIG 4: CNOT gate

3) Double Feynman Gate:
The double Feynman gate is 3*3 reversible gate having inputs (A, B, C) and outputs P=A,Q=A XOR B, R=A XOR C with a quantum cost of 2[8]. The double Feynman can be described as:
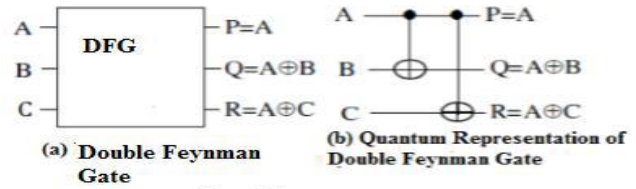

Figure 3.3

4) TOFFOLI Gate:
TOFFOLI gate which is a 3*3 reversible gate with inputs (A, B, C) and outputs P=A, Q=B, R=AB XOR C. It has Quantum cost five [5].
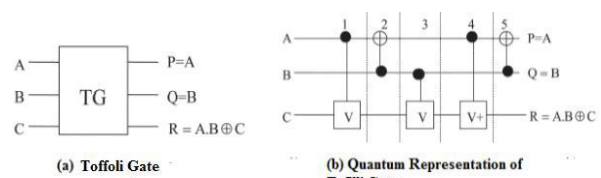

Figure 3.4

5) PERES Gate:
Peres gate which is a 3*3 reversible gate having inputs (A, B, C) and outputs P = A; Q = A XOR B; R = AB XOR C. It has Quantum cost four [6].
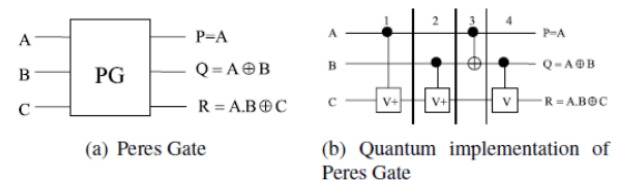

Figure 3.5

6) FREDKIN Gate:
Fredkin gate is a 3*3 reversible gate with inputs (A, B, C) and outputs P=A, Q=A'B+AC, R=AB+A'C. It has Quantum cost five [6].
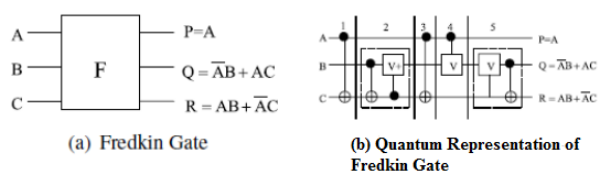

Figure 3.6

7) SAM Gate:
SAM gate is a 3*3 reversible gate with inputs A, B, C and outputs P=A', Q=A'B XOR AC', R=A'C XOR AB. The quantum cost of SAM gate is 4[3].
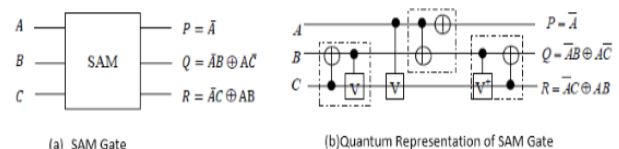

Figure 3.7

II. LITERATURE SURVEY

Reversible Logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Quantum computers are developed using reversible logic circuits. In 1960 R. Landauer showed that, circuits and systems of high technology constructed using irreversible hardware result in energy dissipation due to information loss.

According to him, the loss of one bit of information dissipates at least KTln2 joules of energy, in which K refers to Boltzmann's constant and T is the absolute temperature at which the operation is performed. In 1973 Bennett showed that, one can avoid KTln2 joules of energy dissipation by designing the circuits using reversible logic gates.

[1] An introduction to reversible latches by J E Rice
This paper introduces the details behind two proposed reversible SR latch designs: one design based on the Fredkin gate and one design based on the Toffoli gate. Both of these designs are verified to behave correctly as compared to the traditional, irreversible SR latch and a short comparison is made. We find that the designs are very similar in behaviour, and little can be found to choose between them

[2] A review of reversible logics and it's application in logic design by Nahadi banu and Dibya saha.
This paper presents the primitive reversible gates which are gathered from literature and this paper helps researchers/designers in designing higher complex computing circuits using reversible gates. The paper can further be extended towards the digital design development using reversible logic circuits which are helpful in quantum computing, low power CMOS, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics.

[3] A Distinguish between reversible and conventional logic gates by B Raghu kanth and B murali Krishna.
In this paper, we compared 4-bit reversible adder/ subtractor circuit using DKG gate. Table1 demonstrates the basic comparison of the power and delay for conventional gates and reversible gates Furthermore, the restrictions of reversible circuits were highly avoided. Table2 demonstrates that the comparison is carried out for reversible adder circuit is better than the existing designs in terms of having low power consumption and lesser delay, number of gates, garbage outputs and constant inputs.

[4] Design of sequential circuit element using reversible logic gates by Bhagyalakshmi H R and Venkatesha M K
In this paper an attempt is made to realize the basic sequential elements using two new reversible logic gates namely VB-1 and VB-2. This will help to build more complex reversible sequential circuits.

[5] Comparison of cost metrics for reversible and quantum logic synthesis by Dmitri Maslov and D Micheal miller
The results in Section 5 lead us to the following conclusion. Minimization of Toffoli gate count as a criterion for a reversible synthesis method is not optimal and even for small parameters may result in a seemingly small circuit which may be as far off a technologically favorable implementation as a factor of 8.

It is natural to expect that for circuits with more lines the difference will grow. We suggest that the commonly used gate count metric should be replaced with a metric that accounts for the different costs of large building block (i.e., Toffoli gates), such as the weighted gate cost presented here. Using such a metric would lead to the technologically favorable circuit (b).

[6] Efficient building blocks of reversible sequential circuits and V. Kamakoti
In This paper proposed the design of a new reversible logic gate which is shown to be advantageous for synthesizing multi valued reversible logic. The proposed reversible gate is utilized for efficiently designing the RS latch. The paper proposes the designs of the reversible Flip Flops and Latch using the proposed gate, Fredkin gate, Toffoli and the Feynman gate. The designs are compared with the existing design and are shown to be have an improvement by a factor of 2 to 6. The proposed designs utilized the fact that the reversible circuits constructed from the logic are better in terms of logic complexity and garbage minimization than the one obtained by converting the irreversible designs by replacing gates appropriately. The proposed designs are highly optimized. The number of garbage outputs generated and the number of gates used in the designs are very small as compared to the earlier implementations.

[7] Quantum cost optimization for reversible sequence circuit by Md. Salim al mamun, David menvile.
Reversible latches are going to be the main memory block for the forthcoming quantum devices. In this paper we proposed optimized reversible D latch and JK latches with the help of proposed SAM gates. Appropriate algorithms and theorems are presented to clarify the proposed design and to establish its efficiency. We compared our design with existing ones in literature which claims our success in terms of number of gates, number of garbage outputs and delay. This optimization can contribute significantly in reversible logic community

[8] Optimization of reversible sequence circuit by Aub sadat Md and Masashi ueda.
In this paper we have proposed the reversible design of D-Latch and JK Latch. Latches are important memory element. Thus this optimization will result in great contribution in designing logic circuits with memory and sequential elements. We have given the lower bounds for both the design in terms of number of gates and delay. We have proposed a new reversible gate which can contribute significantly in reversible logic community.

III. APPLICATION

1. The Reversible circuits have application in low power design.
2. Nanotechnology, low power CMOS, optical computing, quantum computer.

IV. CONCLUSION

In this work, I have presented novel designs of reversible D FF with asynchronous set/reset which are optimized in terms of quantum cost, delay and garbage outputs. We conclude that the choice of reversible gates and the design approach to carefully select a reversible gate for implementing a particular logic function will significantly impact the quantum cost, delay and garbage outputs of the reversible design. The application of these FF's as LFSR is designed and discussed. The application of LFSR as pseudo random bit sequence generator is proposed. Further advancement of the proposed work is to use the proposed D FF's towards the designs of complex reversible sequential circuits such as FSM.

REFERENCES

[1] R. Landauer. Irreversibility and heat generation in the computational process. IBM J. Research and Development, 5:183–191, Dec. 1961.
[2] Bennett C.H., "Logical reversibility of Computation", IBM J.Research and Development, pp. 525-532, 1973.
[3] Md. Selim Al Mamun, David Menville Quantum Cost Optimization for Reversible Sequential Circuit, International Journal of Advanced Computer Science and Applications
[4] H. Thapliyal, M. B. Srinivas, and M. Zwolinski. A beginningin the reversible logic synthesis of sequential circuits. In Proc. the Military and Aerospace Programmable Logic Devices Intl. Conf., Washington, Sept. 2005.
[5] E. Fredkin and T. Toffoli. Conservative logic. International J. Theor. Physics, 21:219–253, 1982.
[6] W. N. Hung, X. Song, G.Yang, J.Yang, and M. Perkowski.Optimal synthesis of multiple output boolean functions usinga set of quantum gates by symbolic reachability analysis. IEEE Trans .Computer-Aided Design, 25(9):1652–1663,Sept. 2006.
[7] B.Raghu kanth, B.Murali Krishna, M. Sridhar, V.G. Santhi Swaroop ―A DISTINGUISH BETWEEN REVERSIBLE AND CONVENTIONAL LOGIC GATES ‖, International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 2, Mar-Apr 2012, pp.148-151
[8] Perkowski, M., "A hierarchical approach to computer-aided design of quantum circuits", 6th International Symposium on Representations and Methodology of Future Computing Technology, 201 -209, 2003
[9] M.-L. Chuang and C.-Y. Wang. Synthesis of reversible sequential elements. J. Emerg. Technol. Comput. Syst., 3(4):1–19, 2008.
[10] D. Maslov and D. M. Miller. Comparison of thecost metrics for reversible and quantum logic synthesis. http://arxiv.org/abs/quantph/0511008, 2006.